Customer No.: 31561
Application No.: 10/709,372
Docket NO.: 12409-US-PA

In The Claims:

Claim 1. (currently amended) A non-volatile memory cell, comprising:

a substrate, having a trench thereon;

a gate, formed within the trench;

a first source/drain region, formed at a bottom of the trench;

a composite dielectric layer, formed between the gate and a surface of the trench, wherein the composite dielectric layer comprises at least a charge-trapping layer; ~~and~~

a second source/drain region, formed in the substrate on ~~each~~ one side of the gate.;

and

a third source/drain region located in the substrate on the other side of the gate, wherein the second source/drain region and the third source/drain region are electrically connected to a common bit line.

Claim 2. (original) The non-volatile memory cell of claim 1, wherein the gate completely fills the trench.

Claim 3. (original) The non-volatile memory cell of claim 1, wherein the gate fills the trench and protrudes above the substrate surface.

Claim 4. (original) The non-volatile memory cell of claim 1, wherein the gate further laterally extend above the substrate outside the trench.

Claim 5. (original) The non-volatile memory cell of claim 1, wherein the composite dielectric layer also laterally extend above the substrate outside the trench and positioned between the gate and the substrate.

Claim 6. (original) The non-volatile memory cell of claim 1, wherein the

composite dielectric layer further comprises:

a bottom oxide layer, wherein the charge-trapping layer located between the gate and the bottom oxide layer; and

a cap oxide layer, located between the gate and the charge-trapping layer.

Claim 7. (original) The non-volatile memory cell of claim 1, further comprising spacers formed on the sidewalls of the gate.

Claim 8. (original) The non-volatile memory cell of claim 7, further comprising a lightly doped region formed in the substrate underneath the spacers.

Claim 9. (currently amended) The non-volatile memory cell of claim 1, wherein material constituting the gate comprises doped polysilicon.

Claim 10. (original) The non-volatile memory cell of claim 1, wherein the composite dielectric layer comprises a silicon oxide/silicon nitride/silicon oxide layer.

Claim 11-18. (canceled)